AAYUNA

Advanced Architectures for Scalable Silicon Photonics

A COMPREHENSIVE ANALYSIS OF PASSIVE ALIGNMENT PARADIGMS AND THE AAYUNA OPTICAL INTERCONNECT METHODOLOGY

Executive Summary

The Challenge

The semiconductor industry faces a fundamental bottleneck: as AI workloads drive computational demand to unprecedented levels, the copper interconnects that move data between chips have hit a physical wall. At 112-224 Gbps SerDes speeds, electrical signals can travel only centimeters before degrading, creating a situation where the energy required to move data often exceeds the energy required to compute it. The solution—transitioning to optical interconnects—is well understood. The challenge is manufacturing optical connections at semiconductor scale and cost.

The Opportunity

Co-Packaged Optics (CPO), which integrates optical engines directly into compute packages, represents a multi-billion dollar market opportunity. However, current approaches to fiber-to-chip coupling present a critical tradeoff:

1. **Active alignment** delivers optimal performance but requires $500K+ robotic stations and 5-15 minutes per fiber array—economically unviable at volume
2. **Lens array (expanded beam) solutions** enable passive assembly but sacrifice ~35% of photons (~1.8 dB loss), driving up laser power, thermal load, and system cost

Neither approach scales to the 64-128 optical lanes per package that next-generation AI infrastructure demands.

The AAYUNA Solution

AAYUNA has developed a passive alignment technology that achieves active-alignment-class performance (<0.8 dB loss) without lenses, robots, or proprietary foundry processes. The innovation leverages two mature semiconductor capabilities:

Lithographically defined alignment ridges on the photonic chip, positioned with <100 nm precision relative to waveguides

Anisotropic-etched silicon V-grooves in the fiber carrier, with atomically precise 54.74° sidewalls

When mated, these features create a self-centering mechanical interlock that passively aligns fiber cores to waveguides with micron precision—no active light monitoring required.

Key Differentiators

Metric	Traditional Lens Array	AAYUNA Solution
Insertion Loss	1.5-2.5 dB	<0.8 dB
Assembly Time	5-15 min/FAU	<10 seconds
Equipment CapEx	$500K+ specialized	Standard pick-and-place
Cost	1x	0.3x
Scalability	Linear cost growth	Sub-linear cost growth

Additional Value: Integrated Stiffener

AAYUNA's precision component serves a dual function as a **package stiffener** for CoWoS assemblies. By reinforcing the die edge during reflow, it mitigates the warpage that causes yield loss in advanced 2.5D packages—solving a critical OSAT pain point while creating the optical interface.

Why Now

Three converging factors create urgency:

1. **AI infrastructure demand**: Training frontier models requires thousands of GPUs communicating optically for months; every dB of loss translates to millions in operating cost
2. **CPO adoption acceleration**: Major hyperscalers and switch vendors have committed to CPO roadmaps for 51.2 Tbps+ platforms
3. **Active alignment bottleneck**: At 64-128 lanes per package, no amount of robot speed can achieve required throughput

Competitive Position

1. **vs. TSMC COUPE**: AAYUNA offers foundry-neutral, standards-based approach vs. proprietary vertical integration; comparable or better loss performance at fraction of cost
2. **vs. Lens Arrays**: 50% lower loss, 70% lower CapEx, 30x faster assembly, 50% fewer components
3. **vs. Active Alignment**: Equivalent optical performance with passive assembly economics

Strategic Implications

AAYUNA's technology is designed for ecosystem adoption:

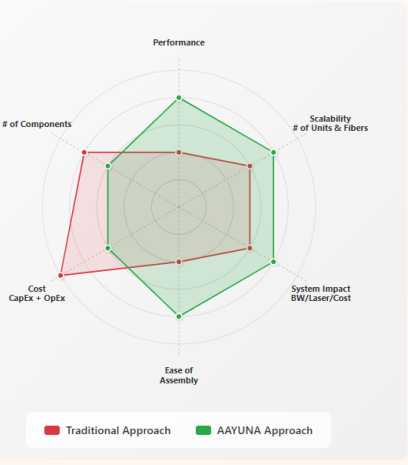
1. **Foundry-neutral**: Alignment ridges use standard lithography/etch available at GlobalFoundries, Intel, Tower, TSMC

2. **PDK-compatible**: Features can be incorporated into existing Process Design Kits

3. **Assembly-friendly**: Compatible with standard OSAT pick-and-place equipment

Companies that control the fiber-to-chip interface will occupy a strategic chokepoint in the AI infrastructure supply chain.

Benefits of Our Approach over the Traditional ones



METRIC	TRADITIONAL COLLIMATED (EXPANDED) BEAM APPROACH	OUR APPROACH
Performance	~1.5-1.8 dB additional loss – perfect fiber mode on the PIC to fiber coupling – Accounting for all the components + assembly tolerances	<0.8 dB additional loss – perfect fiber mode on the PIC to fiber coupling – Accounting for all the components + assembly tolerances ✓
Cost	1x	0.3x ✓
System Impact	3 Interfaces – Laser to PIC + Optical I/O - ~3dB total penalty	Half the number of Lasers (cost/power) or twice the BW ✓
Components	FAU + 2 Lens Arrays (Beam expanders) Collimating + Focusing	FAU + Si V-Grooves Bridge ✓
Assembly	Very high precision alignment of Lens Arrays on both FAU & WGs on the PIC – CapEx + OpEx (UPH)	Simple – Si V-Grooves Bridge self aligns to the Fibers in the FAU & WGs on the PIC ✓
Scalability – No. of Fibers	Assembly complexity increases with the number of Fibers in the FAU	Scales easily with the number Fibers in the FAU ✓
Scalability – No. of Units	Equipment cost & Low UPH (due to # of Degrees of Freedom needed for very precise alignment) increases CapEx & OpEx	Due to self alignment of the Lithography defined precise component with standard way of making FAUs, easily scales ✓

Benefits of AAYUNA's Approach over the Traditional ones. The radar chart shows comparative performance across multiple dimensions including Performance, Scalability, Cost, System Impact, and Ease of Assembly.

Conclusion

AAYUNA has identified and solved the fundamental barrier to scalable Co-Packaged Optics: achieving micron-precision optical alignment using only mechanical features defined by semiconductor lithography. The result is a passive alignment solution that matches active alignment performance at a fraction of the cost, while simultaneously solving the CoWoS warpage challenge that plagues advanced packaging.

As the industry transitions from electrons to photons for short-reach interconnects, AAYUNA's technology provides the missing link between nanometer-precision fabrication and micron-scale fiber assembly. The physics is proven. The economics are compelling. The market is ready.

1. The Interconnect Bottleneck: Physics, Scaling, and the Photons Augmenting the Electrons to Move Data

The semiconductor industry is currently navigating one of the most profound architectural shifts in its history, driven by an inexorable divergence between computational capability and data transport capacity. For over five decades, the industry has operated under the reliable cadence of Moore's Law, doubling transistor density and computational throughput approximately every two years. Today's state-of-the-art logic devices, such as NVIDIA's Blackwell architecture or AMD's Instinct accelerators, integrate well over 100 billion transistors on a single package, enabling exascale computing and the training of trillion-parameter Artificial Intelligence (AI) models. However, while the transistor remains an efficient engine for *processing* information, the copper interconnect, the fundamental mechanism for *moving* that information, has encountered a hard physical barrier known as the "distance-bandwidth product."

The fundamental physics governing electrical transmission lines dictate that as signal frequency increases, attenuation rises non-linearly due to the skin effect and dielectric absorption. In modern data center architectures, SerDes (Serializer/Deserializer) speeds have escalated from 25 Gbps to 56 Gbps and now 112 Gbps PAM4 (Pulse Amplitude Modulation), with 224 Gbps on the immediate horizon. At these frequencies, the effective reach of an electrical signal over a printed circuit board (PCB) trace shrinks from meters to mere centimeters. To compensate for this signal degradation, system architects must employ increasingly complex equalization schemes, re-timers, and forward error correction (FEC) engines. This results in a spiraling power penalty where the energy required to move data across a server rack often exceeds the energy required to compute it. The industry consensus is clear: electrons are ideal for switching logic within the micron-scale confines of a core, but they are increasingly inefficient for transport at the board and rack scale.

The solution to this bottleneck is the transition from electrons to photons for short-reach interconnects. Photons, being bosons with zero rest mass and charge, do not suffer from resistive heating or capacitive loading. Optical fibers have served as the backbone of global telecommunications for forty years precisely because they decouple bandwidth from distance. The challenge facing the industry today is not the physics of optics, but the economics and manufacturability of integrating photonics at the scale and density required by modern silicon. This report analyzes the trajectory of Silicon Photonics (SiPho) packaging, evaluating the limitations of incumbent "active alignment" and "lens array" technologies, and providing a detailed technical deconstruction of the passive alignment solution proposed by AAYUNA Inc. By leveraging the mature ecosystem of the Integrated Circuit (IC) industry, specifically high-precision lithography and anisotropic etching, AAYUNA aims to close the "maturity gap" between electronic and photonic manufacturing.

1.1 The Maturity Gap: Electronics vs. Photonics

The disparity between the electronic and photonic supply chains is not merely one of scale but of fundamental manufacturing philosophy. The IC industry is characterized by monolithic integration, where billions of features are defined simultaneously via photolithography on 300mm silicon wafers. This process is inherently scalable; the marginal cost of an additional transistor is effectively zero. In stark contrast, the traditional optical component industry has historically relied on discrete assembly. Lasers, lenses, isolators, and fibers are often aligned and bonded individually, a process closer to "watchmaking" than semiconductor manufacturing. The investment in IC infrastructure outstrips investment in optics by orders of magnitude.

The primary objective of Silicon Photonics is to democratize optical manufacturing by porting it into the CMOS (Complementary Metal-Oxide-Semiconductor) foundry environment. By fabricating optical waveguides, modulators, and detectors using silicon-on-insulator (SOI) wafers in the same fabs that produce logic chips, the industry leverages the trillions of dollars invested in process control and yield improvement. However, while the *chips* can be printed at scale, the *connection* of those chips to the outside world, specifically, the attachment of optical fibers, remains a stubborn bottleneck that defies standard IC packaging techniques.

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2. Why It Matters: The Business Case for Passive Optical Alignment

2.1 The Inflection Point

The semiconductor industry stands at a critical juncture. The explosive growth of Artificial Intelligence workloads has fundamentally altered the economics of data movement. Training a single frontier AI model now requires thousands of GPUs communicating across optical interconnects for months at a time. Every photon lost at a fiber-to-chip interface translates directly into higher laser power, increased thermal dissipation, and reduced system efficiency. At hyperscale, these inefficiencies compound into millions of dollars in annual operating costs per data center.

The transition from pluggable optics to Co-Packaged Optics (CPO) is no longer a question of "if" but "when." Industry roadmaps project CPO-enabled switches with 51.2 Tbps and beyond within the next product cycles. These systems will require 64 to 128 optical lanes per package—a scale at which traditional assembly methods become economically untenable.

2.2 The Cost of the Status Quo

Active Alignment Economics

Current active alignment systems require multi-axis robotic stages with sub-micron precision, real-time optical power monitoring, and per-channel optimization. The capital equipment cost for a single alignment station exceeds $100,000, with throughput measured in minutes per fiber array. For a CPO module requiring four 32-fiber arrays, alignment alone can consume ~5 minutes of machine time. At

volumes of millions of units per year, this creates a manufacturing bottleneck that no amount of capital investment can fully resolve.

The Lens Array Tax

Expanded beam solutions trade alignment complexity for optical performance. The ~1.8 dB additional loss inherent in lens array interfaces has cascading system-level consequences:

Loss Impact	System Consequence
35% fewer photons reaching the receiver	Higher laser drive current required
Increased laser power	Additional thermal load on package
Thermal management overhead	Larger heatsinks, higher cooling costs
Reduced link margin	Tighter BER budgets, less design flexibility

For a 128-lane CPO module, recovering 1.5 dB of link budget per channel can reduce aggregate laser power by 30-40%, directly translating to lower package thermal design power (TDP) and extended component lifetime.

2.3 Value Creation Across the Ecosystem

For Hyperscalers and Cloud Providers

1. **Power efficiency**: Recovering 35% of lost photons reduces laser power requirements proportionally, contributing to Power Usage Effectiveness (PUE) improvements at facility scale
2. **Bandwidth density**: Lower-loss interfaces enable longer reach at equivalent power, expanding the design space for disaggregated architectures
3. **Reliability**: Elimination of lens arrays removes potential contamination and degradation failure modes
4. **Serviceability**: Passive mechanical alignment enables field-replaceable fiber connections without specialized equipment

For OSATs and Contract Manufacturers

1. **Capital efficiency**: Standard pick-and-place equipment replaces specialized active alignment stations, reducing CapEx by 70% or more
2. **Throughput**: Passive assembly eliminates per-channel optimization, increasing units per hour (UPH) by an order of magnitude
3. **Yield management**: The dual-function stiffener addresses CoWoS warpage—a leading cause of yield loss in advanced packages—while simultaneously creating the optical interface
4. **Process simplicity**: Fewer process steps, fewer failure modes, faster time-to-volume

For Silicon Photonics Foundries and Chip Designers

1. **Foundry neutrality**: Alignment ridges are defined using standard lithography and etch processes available at any CMOS-compatible fab (GlobalFoundries, Intel, Tower, TSMC)
2. **Design portability**: No proprietary process modules required; features can be incorporated into existing Process Design Kits (PDKs)
3. **Reduced integration risk**: Mechanical alignment references are testable at wafer probe, enabling earlier detection of fab excursions

For System Integrators and OEMs

1. **Supply chain flexibility**: Decoupling the fiber interface from foundry-specific processes enables multi-source strategies
2. **Simplified qualification**: Passive mechanical interfaces have deterministic behavior, reducing the test matrix for reliability qualification
3. **Inventory management**: Standardized connectors reduce SKU proliferation across product lines

2.4 Quantifying the Opportunity

Metric	Traditional Lens Array	AAYUNA Passive Solution	Improvement
Assembly CapEx	$100s of K+ per station	Standard pick-and-place	>70% reduction
Alignment time per FAU	2-5 minutes	<10 seconds	>30x faster
Additional insertion loss	1.5-2.5 dB	<0.8 dB	~1 dB
Component count	FAU + 2 lens arrays + focusing optics	FAU + Si V-groove bridge	50% fewer parts
Thermal impact	Higher laser power	Lower laser power	30-40% reduction
Scalability with lane count	Cost grows linearly	Cost grows sub-linearly	Superior at scale

2.5 The Strategic Imperative

The data center industry consumes approximately 1-2% of global electricity, a figure projected to double within the decade as AI workloads proliferate. Every efficiency gain in the optical interconnect – the circulatory system of modern computing – compounds across millions of deployed units.

AAYUNA's passive alignment technology addresses a fundamental constraint in the transition to Co-Packaged Optics: the incompatibility between the nanometer precision of semiconductor manufacturing and the micron-scale tolerances of fiber assembly. By encoding alignment information into lithographically defined mechanical features, the solution transforms optical packaging from an artisanal process into a scalable manufacturing operation.

The companies that solve this integration challenge will define the architecture of next-generation AI infrastructure. The physics is clear. The economics are compelling. The time to act is now.

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3. Historical Context and the Evolution of Silicon Photonics

To understand the significance of current innovations in passive alignment, it is essential to trace the commercial evolution of Silicon Photonics, particularly the pioneering work that established the feasibility of CMOS-compatible optics.

3.1 The Pioneers: Lightwire and Luxtera

In the early 2000s, the concept of manipulating light within silicon waveguides moved from academic research to commercial viability, spearheaded by two seminal companies: **Lightwire** and **Luxtera**. These entities were founded on the premise that the high refractive index contrast between silicon ($n \approx 3.45$) and silicon dioxide ($n \approx 1.45$) could be exploited to create highly confined optical modes, allowing for micron-scale bending radii and dense circuit integration.

Luxtera, a spin-off from the California Institute of Technology (Caltech) founded in 2001, was instrumental in developing "CMOS Photonics." They successfully integrated optical modulators and detectors into a standard CMOS process flow, partnering with TSMC to demonstrate that high-performance optics could be manufactured alongside high-speed electronics. Luxtera's approach involved complex innovations, such as the use of germanium epitaxy for photodetection (since silicon is transparent at infrared wavelengths) and the development of heterogeneous integration techniques for light sources. **Lightwire** pursued a similar path, focusing on carrier-depletion modulators that could operate at high speeds, low power and very high efficiency.

The success of these pioneers was validated by their acquisition by Cisco Systems, Lightwire in 2012 for $271 million and Luxtera in 2019 for $660 million. These acquisitions signaled a strategic shift by major networking vendors to bring optical transceiver technology in-house, recognizing it as a core differentiator for future switch architectures.

3.2 The Persistence of Active Alignment

Despite the success in wafer-level fabrication, the packaging of these early SiPho devices relied heavily on **Active Alignment**. In this process, the optical fiber is brought into proximity with the chip's coupling interface (either an edge coupler or a vertical grating coupler). A laser source is activated, and light is transmitted through the system while a photodetector monitors the output. A high-precision multi-axis robot mechanically manipulates the fiber's position in sub-micron increments to find the point of maximum coupling efficiency (peak power). Once the optimal position is found, the fiber is bonded in place using UV-curable epoxy or solder.

While active alignment delivers high performance by compensating for all geometric tolerances in the system, it is inherently slow and capital-intensive. The cycle time for aligning a single fiber array can range from tens of seconds to minutes, depending on the number of channels and degrees of freedom. As the industry moves toward Co-Packaged Optics (CPO) requiring hundreds of optical I/O ports per package, the linear scaling of alignment time becomes an economic non-starter. The industry urgently requires a transition to **Passive Alignment**, a process where components are placed based purely on mechanical features (fiducials, stops, or keys) without the need for active light monitoring. It is important to have multiple insertion capability to manage yield and Field Service capabilities.

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4. The Physics of Optical Coupling: Challenges and Compromises

The central technical challenge addressed by the AAYUNA whitepaper is the efficient coupling of light between a Single-Mode Fiber (SMF) and a Silicon Photonics Integrated Circuit (PIC). This interface represents the collision of two disparate dimensional worlds: the macroscopic scale of the fiber and the nanoscopic scale of the silicon waveguide.

4.1 The Mode Mismatch Problem

Standard telecommunications fiber (Corning SMF-28) has a core diameter of approximately 8.2 µm and a Mode Field Diameter (MFD) of roughly 9.2 µm at 1310 nm and 10.4 µm at 1550 nm. In contrast, a typical silicon wire waveguide measures roughly 450 nm in width and 220 nm in height to ensure single-mode operation. The optical mode confined within this waveguide is less than 1 μm^2 in cross-sectional area.

Directly "butt coupling" a cleaved fiber to such a waveguide would result in catastrophic coupling loss, typically exceeding ~10 dB (~90% power loss), due to the drastic mismatch in mode size and effective refractive index. To bridge this gap, silicon photonic chips utilize **Spot Size Converters (SSCs)**. These are typically inverse tapers where the silicon waveguide narrows to a sharp tip (e.g., <100 nm wide) or multi-layer nitride waveguides to create the PIC mode very close to the fiber mode. Just 2 µm lateral misalignment can result in an additional loss of ~0.7 dB, necessitating micron precision alignment.

4.2 The Lens Array (Expanded Beam) Paradigm

To relax the stringent lateral alignment tolerances of **SSCs** to Fiber coupling for passive alignment with multiple insertions, the industry has increasingly adopted **Expanded Beam** interconnects using micro-

lens arrays. The principle is straightforward: a lens at the fiber tip collimates the light, expanding the beam diameter to a much larger size (e.g., 50 µm to 100 µm or more) before it crosses the air gap to a matching lens on the chip or connector.

1. **Lateral Tolerance Benefit**: If the beam is expanded to 80 µm, a lateral misalignment of 20 µm represents a small fraction of the total mode area, resulting in negligible coupling loss. This allows for the use of molded plastic lenses and looser mechanical tolerances in the connector body.

2. **The Angular Penalty**: The conservation of the etendue - product of Area×Solid Angle - dictates that expanding the beam diameter must decrease the beam divergence. While this relaxes lateral tolerance, it drastically tightens **angular tolerance**. In an expanded beam system, a tilt of just 0.1 degrees can cause the collimated beam to "walk off" the target lens entirely over a short propagation distance. This shifts the precision requirement from X/Y placement to angular alignment, which can be equally difficult to control in mass production.

4.3 The "~35% Photon Loss" Reality

The AAYUNA whitepaper identifies a critical deficiency in the lens array approach: photon loss. It states that the accumulation of tolerances and additional optical interfaces in lens array solutions results in "losing ~35% of the photons" compared to ideal active alignment. In logarithmic terms, a 35% power loss equates to an insertion loss (IL) of approximately **1.8 dB**.

This figure is consistent with industry data for commercial expanded beam connectors (e.g., standard beam-expanded MPO or MXC connectors), which typically exhibit losses in the range of 1.0 dB to 2.5 dB. While highly optimized research demonstrations, such as TSMC's "EPIC-BOE" presented at IEDM 2024, have achieved additional coupling loss of 1.8 dB in addition to the 0.3 dB of PBSR (Polarization Beam Splitter Rotator) using advanced embedded micro-lenses and grating couplers, these represent the pinnacle of high-cost, integrated foundry processes. Thus, the detachable connectors and standard assembly, the "lens tax" of ~1.5-2.0 dB is a significant burden on the optical power budget, driving up laser power requirements and thermal dissipation.

4.4 Cost and Complexity Drivers

Beyond optical loss, lens array solutions impose significant costs. They require the fabrication and precision assembly of micro-lens arrays on both the fiber side and the chip side. The interface typically involves a complex stack-up:

Waveguide → SSC → Chip Lens → Air Gap → Connector Lens → Fiber

Each interface introduces potential Fresnel reflections (requiring Anti-Reflective coatings) and scattering points. Furthermore, the lenses themselves must often be actively aligned to the waveguides during package assembly, reintroducing the very CapEx problem they were meant to solve.

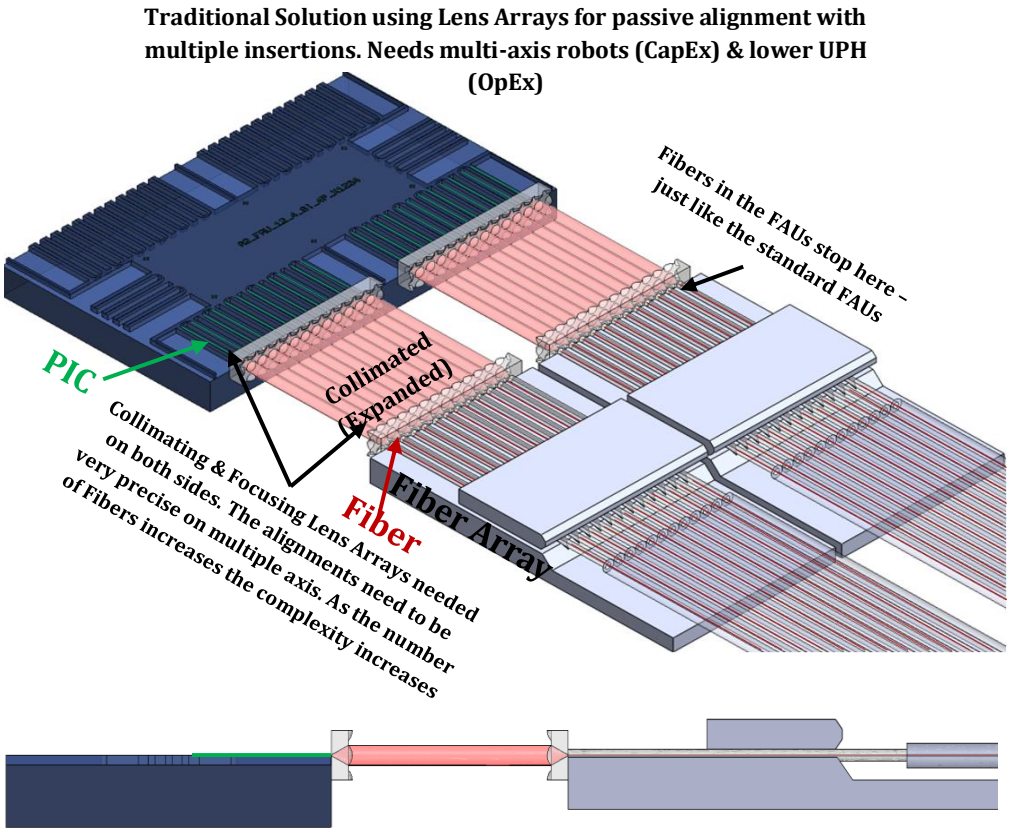

Figure 1: Traditional Solution using Lens Arrays for passive alignment with multiple insertions. Requires multi-axis robots (CapEx) and results in lower UPH (OpEx). Collimating and focusing lens arrays need to be very precisely aligned on both sides, increasing complexity as the number of fibers increases.

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5. The AAYUNA Solution: Passive Alignment via Lithographic Precision

AAYUNA's proposed technology represents a strategic pivot away from optical compensation (lenses) and back to mechanical precision. The core philosophy is to leverage the inherent accuracy of the

semiconductor manufacturing process, specifically lithography and anisotropic etching, to create a "Lego-like" mechanical interlock that guarantees optical alignment by design.

5.1 The Mechanism: Alignment Ridges and V-Grooves

The AAYUNA solution replaces the lens array with a direct, butt-coupled interface enabled by novel mechanical features defined on the chip – part of standard processes in most of the fabs – and the fiber carrier.

5.1.1 Lithographically Defined Alignment Ridges

On the Silicon Photonics (SiPho) die, AAYUNA fabricates "extra-array alignment ridges". These are raised structures or rails located adjacent to the optical waveguide arrays. Because these ridges are defined by the same photolithography mask step that defines the waveguides themselves, the relative distance between the ridge and the waveguide core is fixed with nanometer-scale precision (typically <100 nm error). This effectively transfers the alignment reference from the "optical mode" (which is invisible to a camera) to a "mechanical hard stop" (which can be physically engaged).

5.1.2 Precision V-Grooves

On the fiber side, the fibers are mounted in a Fiber Array Unit (FAU) substrate containing V-grooves. These grooves are etched into single-crystal silicon using anisotropic wet etchants (like Potassium Hydroxide, KOH). This process exploits the crystalline structure of silicon, etching along the crystal planes to form V-grooves with an atomically precise sidewall angle of 54.74°. This ensures that the pitch (spacing) and width of the grooves are controlled to sub-micron tolerances.

5.1.3 The Retracted Fiber Interlock

A key innovation described in AAYUNA's patents is the **retracted fiber** configuration. The optical fibers are bonded into the V-grooves such that the fiber tips are recessed slightly from the front edge of the V-groove carrier. This leaves the front section of the V-grooves empty. During assembly, these empty V-grooves slide into the alignment ridges on the SiPho chip.

1. **Self-Centering Action**: As the ridges engage the V-grooves, the geometry forces the fiber carrier to center itself relative to the chip.

2. **Direct Alignment**: Since the fiber sits in the same V-groove channel that mates with the ridge, and the waveguide is referenced to that same ridge, the fiber core is passively aligned to the waveguide core. This eliminates the need for active light monitoring or complex vision systems.

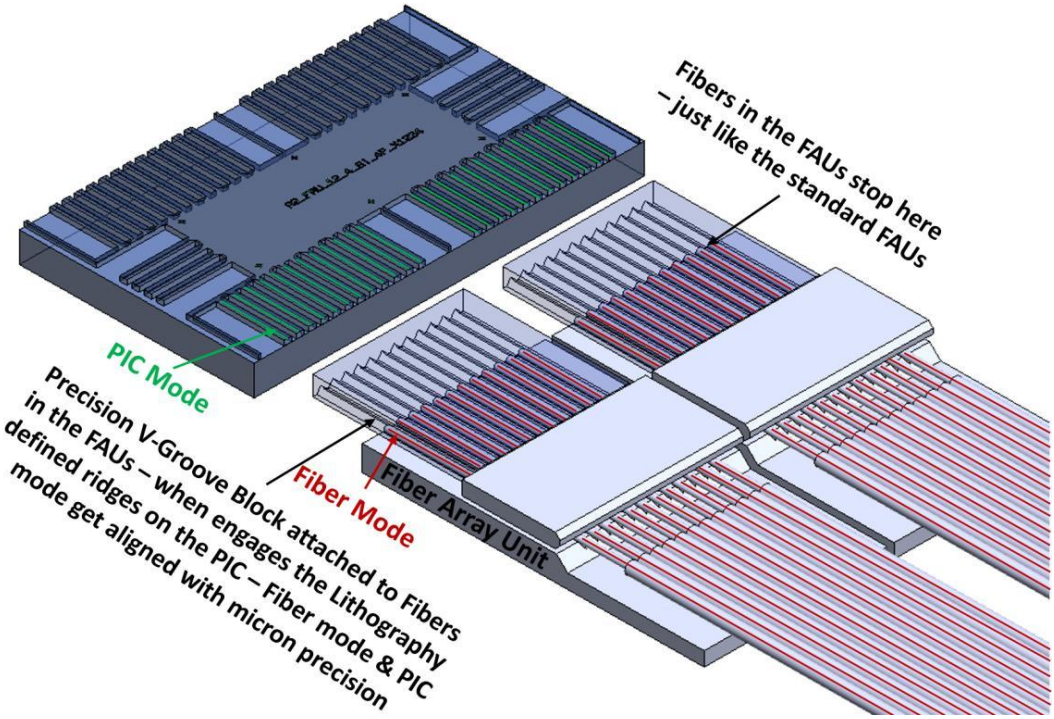

Figure 2: AAYUNA Solution – achieves Micron Precision alignment leveraging the IC industry Ecosystem – Better performance and lower cost. Precision in the FAU's V-Grooves – when Block attaches to Fibers in the FAU, the Litho defined ridges on the PIC get aligned with the Fiber mode with micron precision.

5.2 Leveraging the IC Ecosystem

AAYUNA's approach is predicated on utilizing the mature "IC ecosystem" to achieve precision at scale.

1. **Wafer Dicing**: The whitepaper notes that the IC industry can slice/dice wafers with <3 µm precision. While 3 µm is too coarse for optical alignment, AAYUNA uses dicing only for the gross mechanical outline. The fine alignment is handled by the internal lithographic features (ridges).

2. **Material Uniformity**: By using silicon for both the photonics chip and the fiber connector/receptacle, the system achieves a perfect Coefficient of Thermal Expansion (CTE) match. This is critical for reliability, as it prevents the optical alignment from drifting due to thermal expansion during operation or solder reflow processes.

5.3 Fiber Geometry Tolerances

The viability of this passive approach depends heavily on the geometric consistency of the optical fiber itself. The whitepaper cites a fiber cladding diameter of **125 ± 0.7 µm**.

1. **Historical Context**: In the 1980s, fiber cladding tolerances were as loose as ±3.0 µm, making passive alignment impossible. Modern manufacturing by leaders like Corning and OFS has tightened this to ±0.7 µm or better for standard telecom fibers (SMF-28e+), with "photonic grade" fibers achieving even tighter specs.

2. **Core Concentricity**: A more subtle critical parameter is **Core/Clad Concentricity Error (CCCE)**. Even if the cladding is perfectly aligned by the V-groove, if the core is off-center within the glass, coupling loss will occur. Modern single-mode fibers typically achieve CCCE of <0.5 µm, often <0.2 µm.

3. **Coupling Budget Analysis**: With a V-groove precision of ~0.5 µm and fiber core eccentricity of ~0.5 µm and taking into account the other components assembly tolerances, the worst-case misalignment in a passive system will be less than 2.0 µm. For a standard 9.2-10 µm mode field (butt coupling), this results in <0.8 dB loss. If AAYUNA can maintain these tolerances, their passive solution can rival active alignment performance while vastly undercutting the costs and losses of lens arrays.

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6. The "Stiffener" Innovation: Solving the SiPho IC with TSV Warpage Challenge

AAYUNA's technology proposition extends beyond optical connectivity into the realm of advanced packaging reliability. A significant "second-order" insight from the whitepaper is the dual function of the alignment component as a package stiffener.

6.1 The CoWoS Warpage Challenge

High-performance AI accelerators (GPUs, TPUs) increasingly utilize **Chip-on-Wafer-on-Substrate (CoWoS)** packaging. This 2.5D integration technology places the logic dies and High Bandwidth Memory (HBM) stacks onto a large silicon interposer, which in turn sits on an organic substrate.

1. **The Problem**: These packages are physically large (often >50mm x 50mm) and extremely thin. The organic substrate and the silicon interposer have different Coefficients of Thermal Expansion (CTE). During the solder reflow process (reaching ~260°C), this mismatch causes the entire package to warp or bow.

2. **Impact on Optics**: Warpage is catastrophic for optical edge coupling. If the side of the chip bows by even a few microns, a linear fiber array will fail to couple light uniformly across all channels. Furthermore, warpage induces stress that can crack fragile low-k dielectrics or disconnect Through-Silicon Vias (TSVs).

6.2 The Connector as Structural Reinforcement

AAYUNA proposes attaching the "precision component" (the fiber receptacle) to the SiPho IC at the wafer level. Because this component is made of silicon (or a CTE-matched glass/ceramic), it acts as a rigid beam or **stiffener** along the edge of the die.

1. **Mechanical Stabilization**: By mechanically reinforcing the thinned SiPho die edge, the component mitigates warpage. Dummy stiffeners can be attached as necessary, ensuring the optical interface remains planar.

2. **Process Flow**: This attachment occurs *during* the CoWoS assembly flow. This integration transforms the optical connector from an "afterthought" add-on into an integral structural element of the package, solving a critical mechanical yield problem for the OSAT provider while simultaneously creating the optical port.

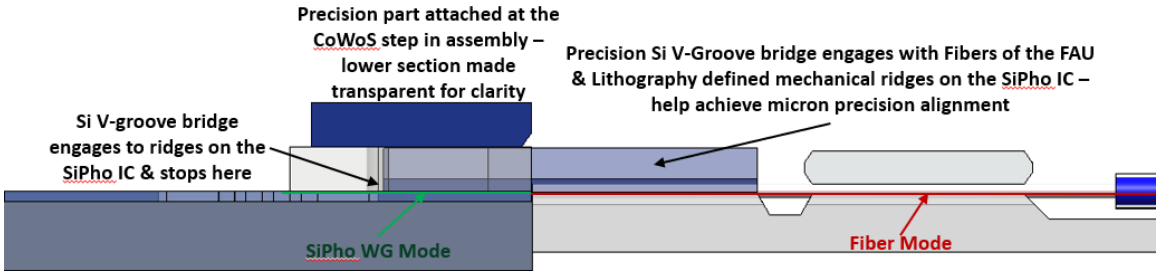

Figure 3: Precision part attached at the CoWoS step in assembly. The Si V-groove bridge engages to ridges on the SiPho IC and stops, while the Precision Si V-Groove bridge engages with Fibers of the FAU and Lithography defined mechanical ridges on the SiPho IC to achieve micron precision alignment.

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7. Industry Landscape and Comparative Analysis

To validate AAYUNA's claims, it is necessary to benchmark their solution against competing industrial approaches.

7.1 TSMC COUPE (Compact Universal Photonic Engine)

TSMC, as the foundry for NVIDIA, AMD, and others, has developed its own vertically integrated solution known as **COUPE** (or EPIC-BOE).

1. **Architecture**: COUPE utilizes 3D stacking (SoIC) where the Electronic IC (EIC) is bonded directly on top of the Photonic IC (PIC).

2. **Optical Coupling**: Recent disclosures at IEDM 2024 describe an "EPIC-BOE" interface using a vertical grating coupler with an embedded micro-lens, achieving additional **1.8 dB coupling loss + 0.3 dB PBSR** (Polarization Beam Splitter Rotation) loss.

3. **Comparison**: TSMC's solution represents the "high road", extreme integration, extreme performance, but proprietary and likely expensive. It relies on internal TSMC process capabilities. AAYUNA's solution is arguably more "foundry-neutral" or "standards-based," relying on physical features (ridges) that can be designed into any CMOS silicon photonics process (GlobalFoundries, Intel, Tower, etc.) and assembled using standard pick-and-place tools. While TSMC achieves loss (~1.8 dB vs AAYUNA's likely <0.8 dB passive target), AAYUNA drastically outperforms the "standard" lens array (1.8 dB) and avoids the proprietary lock-in of COUPE.

7.2 Comparison Table: Optical Coupling Architectures

Feature	Traditional Lens Array (Expanded Beam)	TSMC COUPE (EPIC-BOE)	AAYUNA Passive Solution
Alignment Mechanism	Beam expansion (visual/active)	Integrated Micro-lens + Grating	Mechanical Interlock (Ridges + V-Grooves)
Tolerance Characteristic	Relaxed Lateral / Tight Angular	High Precision Integrated	Precision Mechanical Reference
Insertion Loss (Typical)	~1.5 - 2.5 dB (“35% loss”)	~1.8 dB	< 1 dB (Targeted Passive)
Optical Bandwidth	Broad	Broad with proprietary process	Broad (Edge Coupling)
Polarization	Low Dependence	Additional ~0.3 dB for PBSR	Low Dependence
Packaging Impact	Bulky external connector	3D Stacked Integration	Integrated Stiffener / Edge coupling
CapEx Intensity	High (Active Alignment Robots)	High (Advanced Packaging)	Low (Standard Pick-and-Place)

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8. Future Outlook and Strategic Implications

The trajectory of the data center industry points toward an era of **Co-Packaged Optics (CPO)** where optical engines are no longer pluggable modules on the faceplate but integral components of the compute package.

8.1 The Inevitability of Passive Alignment

As optical lane counts scale from 32 to 64 to 128 per package, active alignment becomes a production bottleneck that no amount of robot speed can solve. The industry *must* move to passive alignment to achieve the necessary volumes. AAYUNA’s approach of shifting the precision burden from the *assembly robot* to the *wafer lithography* is strategically sound. Lithography is essentially “free” precision—it costs the same to print a nanometer-accurate alignment ridge as it does to print a transistor.

8.2 The Ecosystem Play

The success of AAYUNA’s technology will depend on its adoption within the ecosystem. The “alignment ridges” must be supported in the Process Design Kits (PDKs) of major foundries. The process modules are part of standard processing of the PIC. If AAYUNA can standardize these mechanical features, they can create a platform where chip designers simply “drop in” the ridge structure, and packaging houses (OSATs) use standard AAYUNA-compatible fiber connectors to achieve instant, passive, low-loss alignment.

8.3 Conclusion

The AAYUNA whitepaper presents a compelling, physics-grounded solution to the optical interconnect challenge. By rejecting the complexity and loss of lens arrays in favor of high-precision mechanical referencing, it offers a path to scalable, low-loss (<1 dB), and cost-effective Co-Packaged Optics. The innovation of using the optical connector as a mechanical stiffener for CoWoS packages addresses a critical reliability pain point, adding significant value beyond just optical connectivity. As the industry hits the "distance × speed" wall of copper, technologies like AAYUNA's that bridge the gap between the nanometer precision of the fab and the micron scale of the fiber will be the keystones of the next computing era.

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